REMARKS/ARGUMENTS

Spec amendment

[Para 10] and [Para 24] of specification are amended according to examiner's opinion. No new matter is introduced.

Claim amendment

Claim 1 is amended to clearly identify that the operations are performed by the phase-detecting, level-determining device instead of the comparing device. No new matter is introduced.

Claim Rejections – 35 USC 103 (a)

Claims 1-2, 12-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Popplewell et al. (US 6304071) in view of Yamamoto (US 6057730) further in view of Chong et al. (US 7200769).

Response

Claim 1

The applicant appreciates examiner's detail examination, but disagree examiner's opinion, however.

Claim 1 of the applicant's disclosure includes the limitations: " ***a comparing device…for comparing the input signal with the reference level signal and generating the sliced signal according to the result of comparison***". However, the device 4 shown in Fig.1 of Popplewell is an analog to digital converter (ADC), which receives an analogue read signal on an input terminal 8 and provides a digital value Y, representative of the amplitude of the read signal at the rising edge of a clock signal received on a clock input terminal 9, to the phase detector 5 on a first digital line 10 (column 3, line 27~31). That is, the ADC 4 of Popplewell samples the analogue read signal when triggered by the clock signal instead of

comparing the analogue read signal and the clock signal (*emphasis added*). Therefore, the ADC 4 of Popplewell fails to read on the comparing device of the applicant's disclosure and fails to teach or suggest the limitation of "***comparing the input signal with the reference level signal and generating the sliced signal according to the result of comparison***" in claim 1 of applicant's disclosure.

Besides, the phase-detecting, level-determining device in claim 1 of the applicant's disclosure includes the limitations "***detecting the phase at which the transition of the sliced signal occurs***". However, the phase detector 5 of Popplewell provides a phase error value representative of a calculated difference between the actual phase of the clock signal and a desired phase, to the digital loop filer 6 (column 3, lines 31-34) Also, the digital filer 6 of Popplewell operates on the phase error value to provide a filtered phase error value to a DAC 7A (column 3, lines 35~37). Therefore, it is not disclosed that the phase detector 5 and digital filer 6 of Popplewell can detect the phase at which the transition of a signal occurs. Therefore, the combination of these prior art devices fails to disclose the limitation of the phase-detecting, level-determining device in claim 1 of the applicant's disclosure (*emphasis added*).

Furthermore, examiner states that Chong et al. teaches the limitation of the phase-detecting, level-determining device in claim 1 of the applicant's disclosure in (column 8, lines 30~40; figure 3), and Yamamoto teaches the limitation in (column 22, lines 1-15; column 3, lines 45-56). However, Fig.3 of Chong discloses a phase detector 350 and an up/down counter 360. The phase detector 350 determines whether a rising edge of the system clock precedes a rising edge of the delayed clock, and the output thereof is outputted to the up/down counter 360. Also, the output of the up/down counter 360 is outputted to the variable-delay buffer 120 (column 6, lines 17-26). According to the operations detailed in Chong's disclosure (column 6, lines 27-41), after the phase detector 350 detects that the rising edge of the system clock has come before the rising edge of the delayed clock, the up/down counter 360 counts down to reduce the delay through the variable-delay buffers. Oppositely, if the phase detector 350 detects that the rising edge of the system clock has come after the

rising edge of the delayed clock, the up/down counter 360 counts up to increase the delay through the variable-delay buffers.

Therefore, the phase detector 350 of Chong only can determine whether a rising edge of the system clock precedes a rising edge of the delayed clock and the up/down counter 360 increases or reduces the delay value according to the comparing result, but the combination of these prior art devices fails to teach or suggest "***detecting the phase at which the transition of the sliced signal occurs***". Besides, column 8, lines 30~40 of Chong only discloses the phase detector can determine whether a rising edge of the system clock precedes a rising edge of the delayed clock but fails to teach or suggest "***detecting the phase at which the transition of the sliced signal occurs***" in claim 1 of the applicant's disclosure (*emphasis added*), either. According to above-mentioned remarks, the applicant points out that Chong fails to disclose the limitation of the phase-detecting, level-determining device as recited in claim 1 of applicant's disclosure.

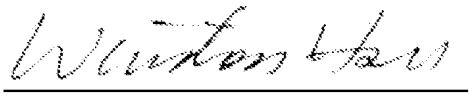
Furthermore, Yamamoto discloses a clock recovery circuit, which compares two sample values, selects a small one thereof, and controls the sampling clock signal so that the amplitude of the smaller one is minimized (column 1 line 61 to column 2, lines 16). Therefore, Yamamoto only discloses comparing two sampled values and improves the signal sampling but fails to teach or suggest "***determine whether a rising edge of the system clock precedes a rising edge of the delayed clock***" in claim 1 of the applicant's disclosure (*emphasis added*).

According to above-mentioned remarks, Popplewell, Yamamoto and Chong all fail to disclose the limitations in claim 1 of the applicant's disclosure. Claim 1 of the applicant's disclosure is not disclosed even these cited references are reasonably combined. Thus the rejection of claim 1 under 35 U.S.C. 103(a) should be overcome.

Claims 2 and 10-17 are dependent upon claim 1, and should be allowed if claim 1 is found allowable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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